Exam

Name_____

TRUE/FALSE. Write 'T' if the statement is true and 'F' if the statement is false.

1) The values of an analog signal flow smoothly from one to the next. 1) _____

2) A sinusoidal waveform is an analog signal. 2) _____

3) Digital data can be processed and transmitted more efficiently and reliably than analog information. 3) _____

4) The field that comprises both mechanical and electronic components is known as electro-mechanics. 4) _____

5) The decimal number system uses nine different symbols. 5) _____

6) The binary number system uses just two symbols. 6) _____

7) A waveform that repeats itself at fixed intervals is called a *periodic* waveform. 7) _____

8) Digital systems respond to voltage levels that change abruptly between two levels (high and low). 8) _____

9) The amplitude of a digital waveform is the difference in voltage between the LOW and HIGH levels. 9) _____

10) The clock signal synchronizes the other waveforms in a circuit. 10) _____

11) Clock signals carry pieces of information such as letters and numbers. 11) _____

12) Serial data is sent along a single conductor, one bit at a time. 12) _____

13) Parallel data is sent along a single conductor, one bit at a time. 13) _____

14) When the inputs to a 2-input AND gate are both HIGH, the output is HIGH. 14) _____

15) When either input to a 2-input AND gate is LOW, the output is LOW. 15) _____

16) When either input to a 2-input OR gate is HIGH, the output is HIGH. 16) _____

17) When both inputs to a 2-input OR gate are both LOW, the output is LOW. 17) _____

18) When the input to a logic inverter is HIGH, the output is LOW. 18) _____

19) Encoders and decoders perform opposite conversions. 19) _____

20) A multiplexer converts parallel data to serial data. 20) _____

21) A demultiplexer is sometimes called a *mux*. 21) _____

22) A flip-flop is a 1-bit storage device. 22) _____

23) The DIP package style has two parallel rows of through-hole pins. 23) _____

24) The PLCC package has J-type leads on all four edges. 24) _____

25) The flat-pack (FP) IC package style is a surface-mount device. 25) _____

26) The FPGA is a fixed-function device. 26) _____

MULTIPLE CHOICE. Choose the one alternative that best completes the statement or answers the question.

27) A circuit that converts an analog waveform to a digital signal is commonly called a(n) _____. 27) _____
A) PLD B) ADC C) CAD D) DAC

28) A circuit that converts an digital signal to an analog waveform is commonly called a(n) _____. 28) _____
A) PLD B) CAD C) ADC D) DAC

29) Of the circuits listed, the one that is most likely to be found in a CD player is a(n) _____. 29) _____
A) SPLD B) programmable logic device
C) digital-to-analog converter D) analog-to-digital converter

30) On a negative-going pulse, _____. 30) _____
A) HIGH = 0 and LOW = 1 B) HIGH = 0 and LOW = -1
C) HIGH = 1 and LOW = 0 D) LOW = -1 and HIGH = 1

31) On a digital waveform, the transition time from a LOW level to a HIGH level is called _____. 31) _____
A) period B) rise time C) pulse width D) fall time

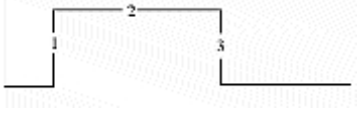


Figure 1-1

32) Which edge in Figure 1-1 is the leading edge? 32) _____
A) 1 B) 2 C) 3 D) Both 1 and 3

33) Which edge in Figure 1-1 is the trailing edge? 33) _____
A) 1 B) 2 C) 3 D) Both 1 and 3

34) The time between transition 1 and transition 3 in Figure 1-1 is the _____. 34) _____
A) frequency B) pulse width C) amplitude D) period

35) On a digital waveform, the transition time from a HIGH level to a LOW level is called _____. 35) _____
A) rise time B) period C) fall time D) pulse width

36) The time from one leading edge on a digital waveform to the next is the waveform _____. 36) _____
A) pulse width B) fall time C) rise time D) period

37) A periodic digital waveform _____. 37) _____
A) has a duty cycle
B) repeats itself at a fixed interval
C) has both a HIGH and LOW levels
D) all of the above

38) The transition times for an ideal digital pulse are _____. 38) _____
A) measured between 0 and 90% of the amplitude
B) zero
C) measured between 10% to 90% of the amplitude
D) infinite

39) An oscilloscope display indicates that the period of a digital waveform is 40 µs. What is frequency of this waveform? 39) _____
A) 25 kHz
B) 2.5 kHz
C) 40 MHz
D) The frequency cannot be determined using the information provided.

40) What is the duty cycle of a digital waveform with a pulse width of 10 ms a period of 90 ms? 40) _____
A) 11.1% B) 9% C) 90% D) 10%

41) On a positive-going pulse, the leading edge is the _____. 41) _____
A) HIGH-to-LOW transition
B) positive-going edge
C) negative-going edge
D) falling edge

42) The approximate duty cycle for the digital waveform below is _____. 42) _____

A) 50% B) 80% C) 30% D) 20%

43) On a negative-going pulse, the leading edge is the _____. 43) _____
A) LOW-to-HIGH transition
B) rising edge
C) negative-going edge
D) positive-going edge

44) On a positive-logic pulse, the trailing edge is the _____. 44) _____
A) positive-going edge
B) rising edge
C) falling edge
D) LOW-to-HIGH transition

45) On a negative-logic pulse, the trailing edge is the _____. 45) _____
A) positive-going edge
B) negative-going edge
C) falling edge
D) HIGH-to-LOW transition

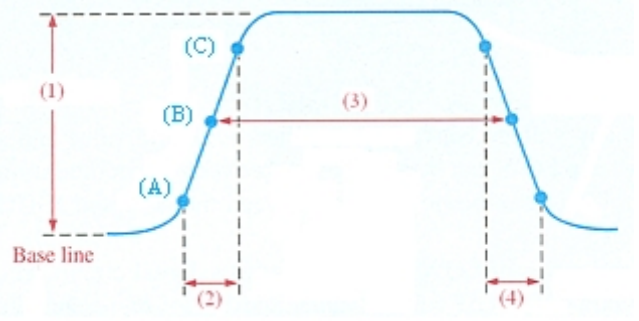


Figure 1-2

46) Item (1) of the nonideal pulse in Figure 1-2 represents the waveform _____. 46) _____
A) period B) amplitude C) transition time D) pulse width

47) Item (2) of the nonideal pulse in Figure 1-2 represents the waveform _____. 47) _____
A) amplitude B) rise time C) fall time D) pulse width

48) Item (3) of the nonideal pulse in Figure 1-2 represents the waveform _____. 48) _____
A) amplitude B) rise time C) fall time D) pulse width

49) Item (4) of the nonideal pulse in Figure 1-2 represents the waveform _____. 49) _____
A) amplitude B) rise time C) fall time D) pulse width

50) When data is set along a single conductor, it is referred to as _____. 50) _____
A) parallel data B) serial data
C) simultaneous data D) none of these

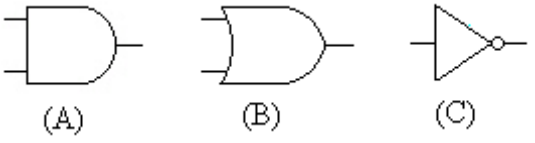


Figure 1-3

51) The symbol in Figure 1-3(A) represents the _____ function. 51) _____
A) OR B) NOT C) AND D) AND/OR

52) The symbol in Figure 1-3(B) represents the _____ function. 52) _____
A) NON B) OR C) AND D) XOR

53) The symbol in Figure 1-3(C) represents the _____ function. 53) _____
A) XOR B) NOT C) AND D) OR

54) The output from an AND gate is HIGH when _____. 54) _____
A) all inputs are HIGH
B) one input is LOW and the remaining inputs are HIGH
C) one input is HIGH and the remaining inputs are LOW
D) all inputs are LOW

55) The output from an AND gate is LOW _____. 55) _____
A) only when all inputs are HIGH B) when at least one input is LOW
C) only when all inputs are LOW D) none of the above

56) The output from an OR gate is HIGH _____. 56) _____
A) only when all inputs are LOW B) only when all inputs are HIGH
C) when at least one input is HIGH D) none of the above

57) The output from an OR gate is LOW _____. 57) _____
A) whenever any input is HIGH B) only when all inputs are HIGH
C) only when all inputs are LOW D) none of the above

58) Which circuit creates an output that indicates whether or not the input values are equal? 58) _____
A) Comparator B) Encoder C) Decoder D) Multiplexer

59) Which circuit converts information into a specific coded form? 59) _____
A) Comparator B) Encoder C) Decoder D) Multiplexer

60) Which circuit converts coded information into a noncoded form? 60) _____
A) Comparator B) Encoder C) Decoder D) Multiplexer

61) Which circuit converts data from serial form to parallel form? 61) _____
A) Demultiplexer B) Encoder C) Comparator D) Multiplexer

62) Which one of the following is not a binary arithmetic function? 62) _____
A) Division B) Addition C) Multiplexing D) Subtraction

63) Two kinds of data selectors are _____ and _____. 63) _____
A) adders, subtractors B) multiplexers, demultiplexers
C) encoders, decoders D) comparators, registers

64) Which one of the circuits listed is made up of flip-flops? 64) _____
A) A converter B) A register C) A multiplexer D) A comparator

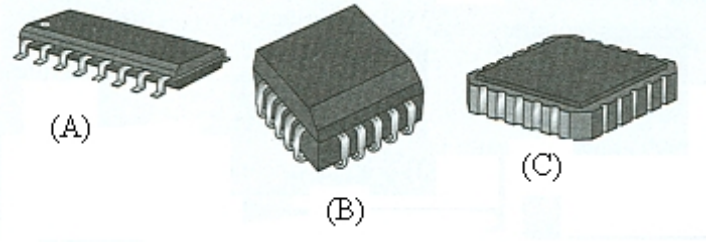


Figure 1-4

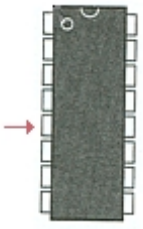
65) The package style in Figure 1-4(A) is a(n) _____. 65) _____
A) SOIC B) PLCC C) LCCC D) FP

66) The package style in Figure 1-4(B) is a(n) _____. 66) _____
A) SOIC B) PLCC C) LCCC D) FP

67) The package style in Figure 1-4(C) is a(n) _____. 67) _____

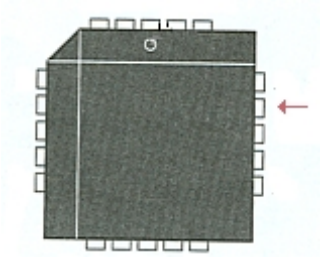
A) SOIC B) PLCC C) LCCC D) FP

68) The arrow in the figure below points to pin number _____. 68) _____



A) 5 B) 4 C) 13 D) 12

69) The arrow in the figure below points to pin _____. 69) _____



A) 4 B) 17 C) 16 D) 5

70) Which IC package style has no leads? 70) _____

A) SOIC B) LCCC

C) PLCC D) All must have leads.

71) Which one of the following is not a surface-mount IC package? 71) _____

A) FP B) DIP C) PLCC D) SOIC

72) The first step in the PLD programming process is _____. 72) _____

A) design entry B) compilation C) synthesis D) download

73) The final step in the PLD programming process is _____. 73) _____

A) design entry B) compilation C) synthesis D) download

74) The netlist is generated during the _____ phase of the PLD programming process. 74) _____

A) design entry B) compilation C) synthesis D) download

75) Which of the following is an example of a mechatronics system? 75) _____

A) An industrial robot B) A surgical laser

C) A laptop computer D) None of the above

Answer Key
Testname: UNTITLED1

1) TRUE
2) TRUE
3) TRUE
4) FALSE
5) FALSE
6) TRUE
7) TRUE
8) TRUE
9) TRUE
10) TRUE
11) FALSE
12) TRUE
13) FALSE
14) TRUE
15) TRUE
16) TRUE
17) TRUE
18) TRUE
19) TRUE
20) TRUE
21) FALSE
22) TRUE
23) TRUE
24) TRUE
25) TRUE
26) FALSE
27) B
28) D
29) C
30) A
31) B
32) A
33) C
34) B
35) C
36) D
37) D
38) B
39) A
40) A
41) B
42) D
43) C
44) C
45) A
46) B
47) B
48) D
49) C
50) B

51) C
52) B
53) B
54) A
55) B
56) C
57) C
58) A
59) B
60) C
61) A
62) C
63) B
64) B
65) A
66) B
67) C
68) A
69) B
70) B
71) B
72) A
73) D
74) C
75) A